SXGA060 Series
Low-Power AMOLED Microdisplay

Data Sheet

Pre-Spec V0.1

SXGA060SC   SXGA060SW   SXGA060SG

For Products:

SXGA060SC   —   Full Color
SXGA060SW   —   Monochrome White
SXGA060SG   —   Monochrome Green

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Record of Revision

Version	Revise Date	Page	Content
Pre-spec. V1.0	2013-07		Initial release.

Contents

1 FEATURES

1.1 Description

- Si-Base AMOLED Microdisplay
  - 0.18μm CMOS Technology
  - Full Digital Video Core
  - High Efficiency Top Emission Structure
  - Low Power Consumption
- 1280×1024 (SXGA) Resolution
  - View Area: 0.6 inch
  - Pixel Pitch : 9.3μm
  - Total Pixels : 1284 (×3)× 1028
- Digital Video Interface
  - Compatible with ITU-R BT.656/601
  - Accept 8/16/24-Bit Digital Video
  - Accept YCbCr/RGB Color or Mono
  - Support SXGA/XGA/SVGA/VGA etc
  - Support DDR/SDR Mode

- Digital Video Signal Enhancement
  - Brightness
  - Contrast
- Gamma Correction
  - Asyn10Bit 256Level RGB Separated Gamma LUT
  - Expand 8bits Input to 10bits Output
- Full Scale 10-Bit DAC
- Support Binocular Stereovision
- Horizontal/Vertical Mirror
- Shift and Position Control
- Embed Temperature Sensor
- Integrate 9-Bit ProgrammableVcom Module
- Built-in Test Patterns
- 2-Wire Series Interface
- Single 5V Power Supply

1.2 Products Coding

<div align="center">

SXGA   060   S   C   V1   R1

①   ②   ③   ④   ⑤   ⑥

</div>

①Type	
SVGA	800x600
SXGA	1280x1024

③Temperature	
S	Standard: -40 ～ +65℃
N	Normal: -10 ～ +40℃

⑤Connector	
V1	Board to Board
V2	FPC

②Size	
050	0.5 Inch
060	0.6 Inch
097	0.97 Inch

④Color	
C	Full Color
W	Mono White
G	Mono Green

⑥Revision	
R1	Revision No.

2 INTRODUCTION

SXGA060 series AMOLED microdisplay fabricated by OLiGHTEK's proprietary top emitting and high luminance efficiency Si-Base AMOLED technology. SXGA060 series microdisplay includes full color, Monochrome white, Monochrome green and other specifications. With the same interface and pin definition, SXGA060 series products have 11.941mm×9.560mm (0.6 inch) display area, and supported less than or equal to SXGA resolutions format. With proper optic enhancement devices, the microdisplay can provide high quality, large virtual image.

SXGA060 series microdisplay's silicon substrate is fabricated by 0.18μm CMOS technology, integrated full digital video signal processing, 1284×1028×3 active driving units, digital logic control, scan distribution, D/A converting, temperature sensor, gamma correction, DC-DC for cathode's negative voltage, two-wire serial communication interface and so on. The input video signal is compatible with ITU-R BT. 656/601 and support 8/16/24 bits digital video. The function of microdisplay such as display mode, scanning direction, display position, brightness, contrast and gamma correction can be programmed through the two-wire serial communication interface. The digital interface voltage level is compatible with 1.8~3.3V CMOS standard. The microdisplay operate on a signal 5V power supply and can be applied in various near-to-eye display systems that demand compact size, high resolution, low power consumption and wide working temperature range.

2.1 Characteristic Parameters

| Model	SXGA060		
Product Type	Color	Monochrome White	Monochrome Green
Resolution	1280 (×3) × 1024		
Active pixels	1284 (×3) × 1028		
Pixel Aspect Ratio	1:1		
Color Pixel Arrangement	RGB Vertical Stripe		
Gray Levels	8bits/256Levels, 10bits/1024Levels		
Gamma Correction LUT	3×256×10Bit		
Luminance Uniformity	> 90%		
Contrast	> 10000:1		
Digital Video Interface	ITU-R BT.601/656 24-bit，4:4:4，RGB/YCbCr 16-bit，4:2:2，YCbCr 8-bit，4:2:2，YCbCr/Mono		
Operating Temperature	Standard	-40℃ ～ +65℃	
	Normal	-10℃ ～ +40℃	
Chromaticity	White	CIEx=0.30±0.05, CIEy=0.35±0.05	
	Green	CIEx=0.30±0.05, CIEy=0.63±0.05	
Operating Humidity	≤85%RH (Non condensing)		
Pixel Size(μm²)	9.3 × 9.3		
Viewing Area(mm²)	11.941× 9.560		
Mechanical Envelope(mm³)	22 × 17 × 5.2		
Operating Luminance(Cd/m²)	>70	>100	
Operating Power Consumption(mW)	<000	<200	
Lifetime(Hours)	25000	25000	
Power Supply	DC 5.0V@Max200mA		
Weight(g)			

2.2 Product Structure
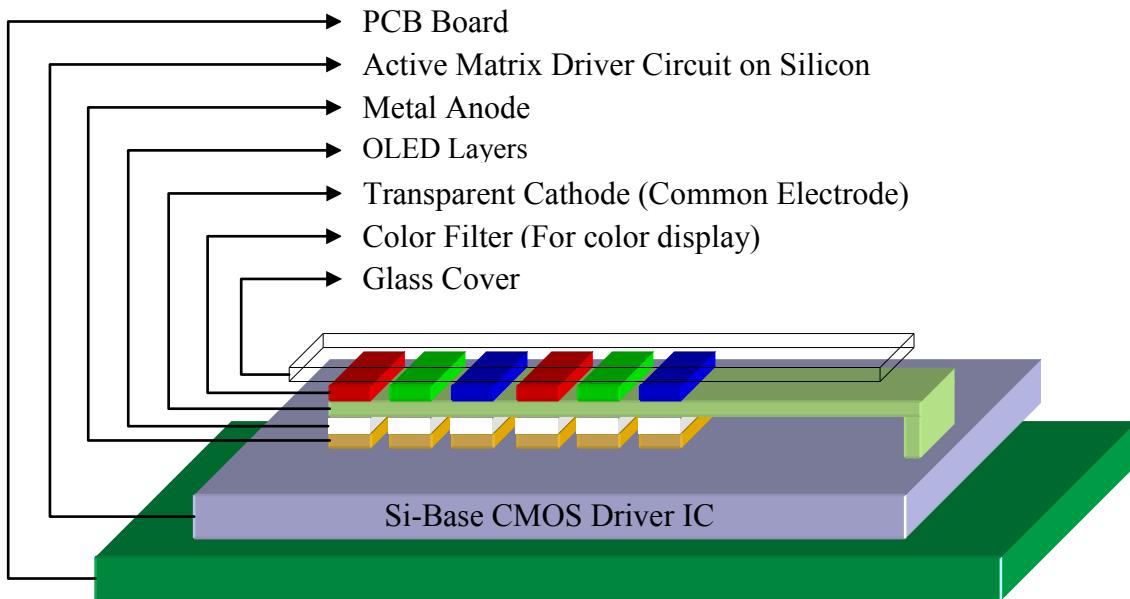
Figure 2-1   SXGA060 series device's structure

OLiGHTEK's SXGA060 series AMOLED microdisplay is manufactured on a silicon substrate which is integrated with video signal processing and active driver, then followed by sub-pixel metal anode, multi-layer OLED light-emitting film, transparent cathode(common cathode), compound high density sealing film, RGB color filter layer, etc., after which paste glass cover to protect the microdisplay, and bond with PCB board. Figure 2-1 shows the device's structure.

2.3 Pixel Array
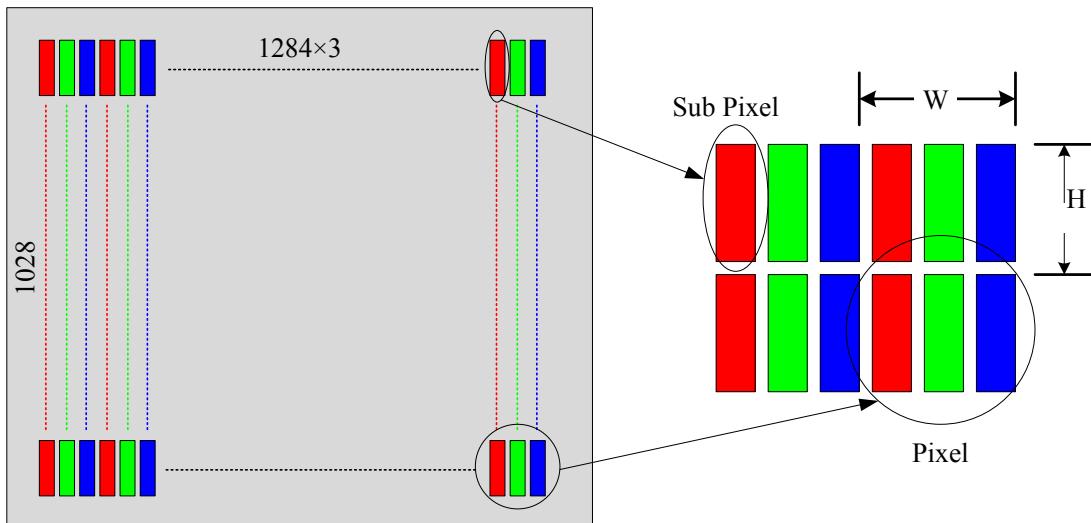
Figure 2-2   Pixel and Sub-Pixel Array

Each pixel of OLiGHTEK's SXGA060 series AMOLED microdisplay is formed by three sub-pixels (Figure 2-2). The pixel's related parameters are shown below:

Model	Pixel Size		Duty Cycle	View Area	
	Width(W)	Height(H)		Width（1284×W）	Height（1028×H）
SXGA060	9.3μm	9.3μm	68%	11.941mm	9.560mm

Each sub-pixel of colorful display emits white light, and full-color display is fulfilled through the RGB color filter. Since there is no color filter, the luminous efficiency of the monochrome display is higher than the color display.

2.4 Function Diagram
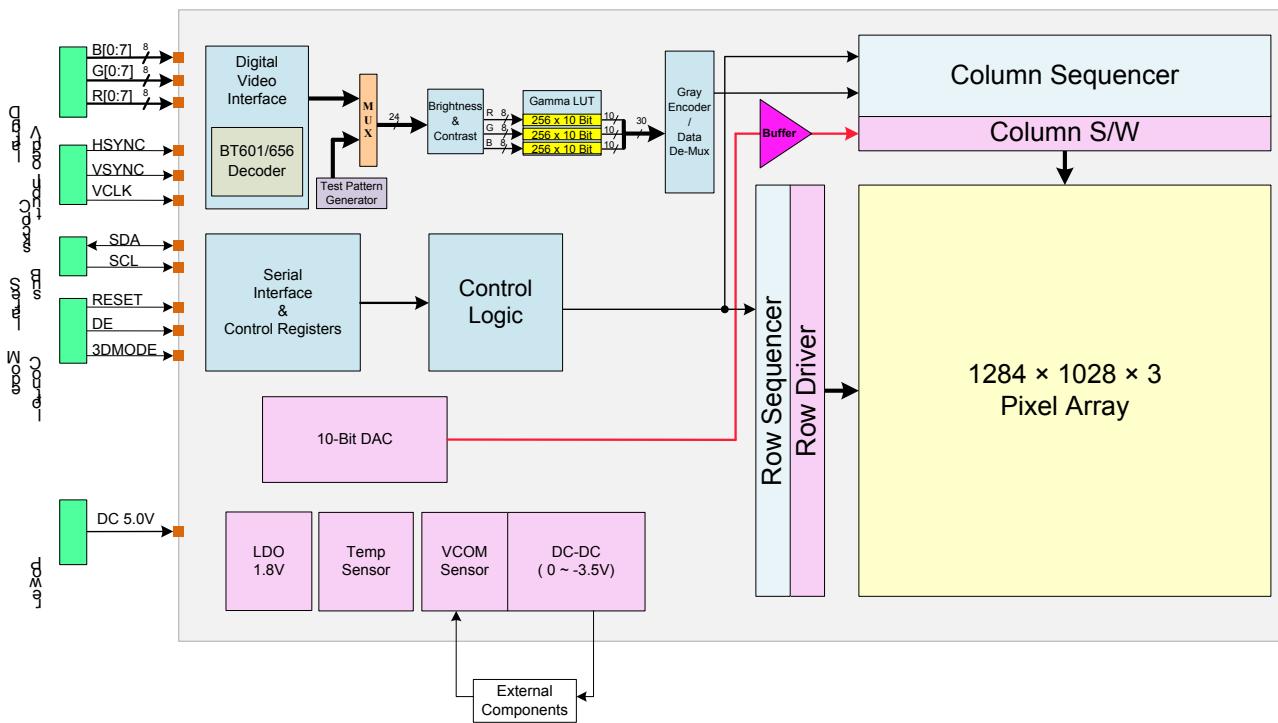
Figure 2-3   SXGA060 Series Architecture & Principle Diagram

Figure 2-3 shows top level block diagram of SXGA060 series microdisplay's driver circuit. The chip is mainly composed of the digital video signal interface and decoder, digital video signal processing, digital Gamma correction, gray mapping, D/A conversion, row & column scanning, pixel driver array, two-wire serial communication interface, programmable control logical unit, temperature sensor, DC/DC converter and other function modules.

Compatible with ITU-R BT.656/601 standards, digital video signal interface has three 8-bit data channels and accepts 8/16/24 bits RGB or YCbCr video signals. According to the different input formats, the internal video decoder outputs 24 bits RGB signal always. The digital video signal processing circuit receives the 24 bits RGB signal, and then adjusts the brightness, contrast respectively. The output signal is still 24 bits format and sent to the gamma correction circuit. The gamma correction circuit makes corrections of the 24 bit RGB signal by separated RGB look-up table, and extends it to 30 bits RGB signal output. By D/A conversion, the gray mapping circuit converts the three 10 bit R/G/B signals to three R/G/B analog voltage signals. The voltage stands for the R,G,B luminance, Then, the analog signal is stored in sub-pixel driving unit; driving unit circuit applies the RGB analog voltage signal to OLED's anode and holds the voltage on for one frame/field cycle time. With external 5V power supply and external components on PCB backplane, the DC/DC module generates a negative voltage which is applied to all of the OLED sub-pixels' common cathode. Under the bias voltage between the anode and the cathode, OLED keeps emitting light in one whole frame/field cycle.

Through the internal programmable SRAM (register), control logic unit deals with the digital signal, makes the different unit circuits working in harmony with each other, and realizes the binocular 3D display.

Compatible with I^{2}C communication standard, the two-wire serial interface is used to realize the read/write operation of the registers, accordingly, make the chip circuit programmable, such as digital video signal decoding and processing, gamma correction, DC/DC conversion and so on.

The internal temperature sensor circuit updates the corresponding register's numeral value which represents the real-time internal working temperature. The numeral value is read by the external control logic unit through the two-wire serial interface. According to the luminance-temperature character, OLED's common cathode's negative voltage can be adjusted by DC/DC converter so as to get proper luminance at different temperatures.

2.5 Interface & Pin Assignment

2.5.1 Connector & Pin Assignment

SXGA060-V1 series microdisplay use a 0.5mm pitch, 40pins connector made by Hirose, part number is DF12D(3.0)-40DP-0.5. SXGA060-V1 keeps pin-compatibility with SVGA-V1.
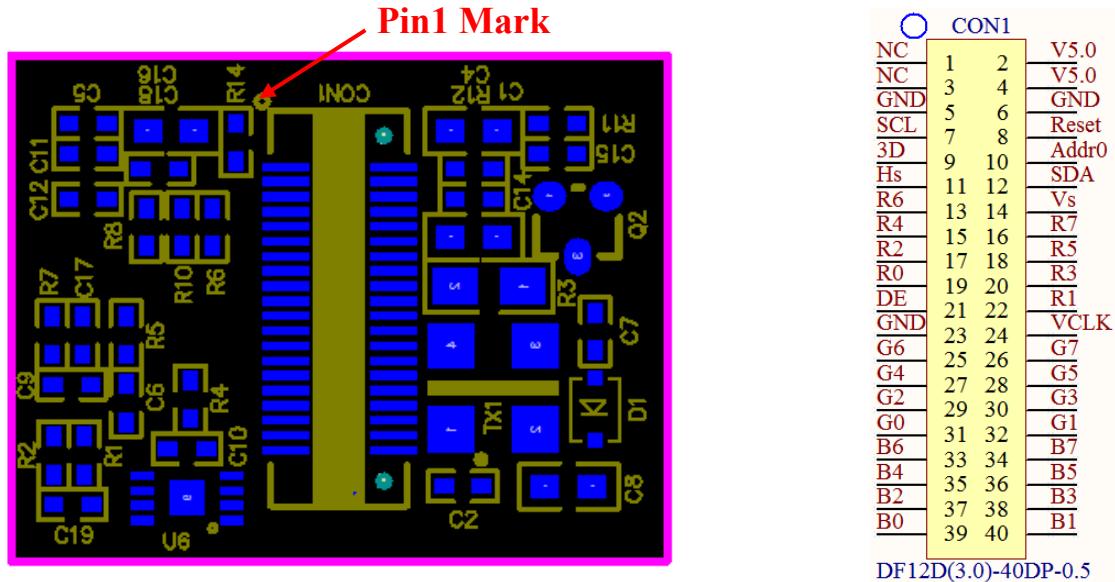

Figure 2-4   SXGA060 series microdisplay connector & pin assignment

2.5.2 Pin Definition

Pin	Symbol	I/O	Function	Remark	Pin	Symbol	I/O	Function	Remark
1	NC	-	Not used		2	V5.0	P	5.0V Power Suppply	
3	NC	-	Not used		4	V5.0	P	5.0V Power Suppply	
5	GND	P	Power ground		6	GND	P	Power ground	
7	SCL	I	Serial Port Clock Line	Pull-up 1.8V	8	Reset	I	Master Reset, Active Low	Can't Floating
9	3D	I	3D L/R Signal Input		10	Addr0	I	Serial Port Address A0	Pull-up 1.8V
11	Hs	I	Hsync Signal Input		12	SDA	I/O	Serial Port Data Line	Pull-up 1.8V
13	R6	I	Video Data Input R[6]		14	Vs	I	Vsync Signal Input	
15	R4	I	Video Data Input R[4]		16	R7	I	Video Data Input R[7]_MSB	
17	R2	I	Video Data Input R[2]		18	R5	I	Video Data Input R[5]	
19	R0	I	Video Data Input R[0]_LSB		20	R3	I	Video Data Input R[3]	
21	DE	I	Data Enabl Signal Input		22	R1	I	Video Data Input R[1]	
23	GND	P	Power ground		24	VCLK	I	Pixel Clock Input	
25	G6	I	Video Data Input G[6]		26	G7	I	Video Data Input G[7]_MSB	
27	G4	I	Video Data Input G[4]		28	G5	I	Video Data Input G[5]	
29	G2	I	Video Data Input G[2]		30	G3	I	Video Data Input G[3]	
31	G0	I	ideo Data Input G[0]_LSB		32	Gl	I	Video Data Input G[1]	
33	B6	I	Video Data Input B[6]		34	B7	I	Video Data Input B[7]_MSB	
35	B4	I	Video Data Input B[4]		36	B5	I	Video Data Input B[5]	
37	B2	I	Video Data Input B[2]		38	B3	I	Video Data Input B[3]	
39	B0	I	Video Data Input B[0]_LSB		40	B1	I	Video Data Input B[1]	

2.6 Recommended Operation Ratings

SYMBOL	DESCRIPTION	MIN	TYP	MAX[①]	UNIT
V5.0	5.0V Power Supply	4.5	5.0	6.0	V
$V_{I/O}$	Digital Signal Voltage[②]	—	1.8	3.3	V
Tstorage	Storage Temperature	-55	20	90	°C
Toperate	Operation Temperature	-40	20	65	°C

Note ①: The absolute maximum rating values (except $V_{I/O}$) of this product are not allowed to be exceeded at any time. If the product is used with its symbol value exceeding the maximum rating or in an extreme condition, the characteristics of the device maybe recovered and the lifetime of the device will decrease, even the device may be permanently destroyed.

Note ②: All the Digital logic Pins (except the Power Pin) can support 1.8V/3.3V CMOS logic level.

2.7 Electrical Characteristics

2.7.1 DC Characteristics

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{5.0}$	5.0V Supply Current		10	40	200	mA
Vcom	Cathode Voltage		-3.5	-2	0	V
Typical Power Consumption	Working	Color @ 70Cd/m2	80	120	200	mW
		Monochrome White @ 100Cd/m2	60	100	200	
		Monochrome Green @ 1500Cd/m2				
	Display Off		40	-	60	
	Power Down		0.4	-	2	

2.7.2 AC Characteristics
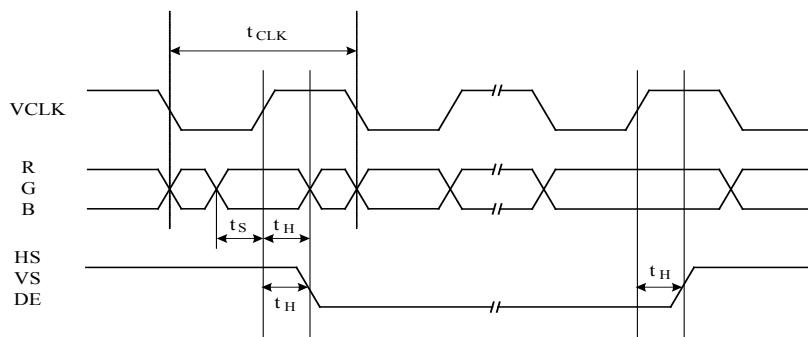
PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Digital Video Data Setup & Hold	t_S	1	-	-	ns
	t_H	1	-	-	ns
Video Clock Period	t_{CLK}	4.6	-	-	ns
Video Clock Duty	q	40	50	60	%

3 DETAILED FUNCTION DESCRIPTION

3.1 Digital Video Interface
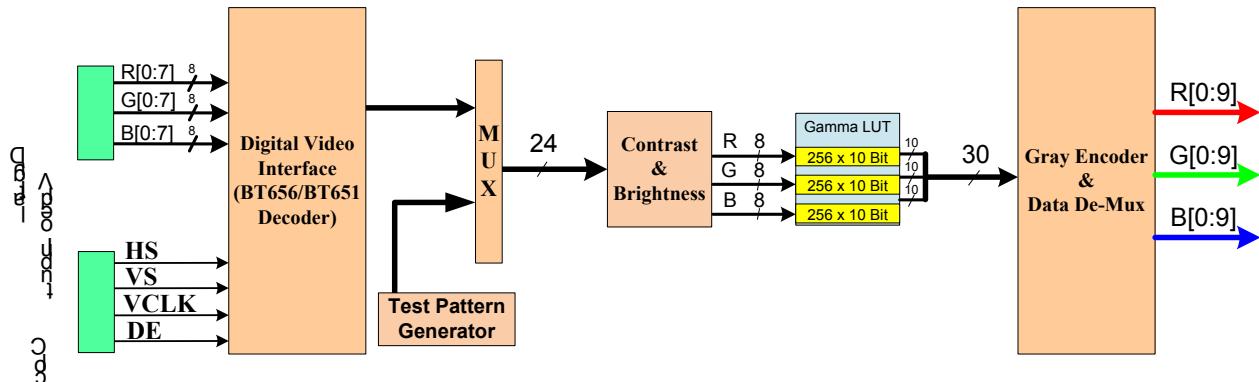
Figure 3-1   Digital Video Processing Flow Diagram

The digital video interface has three 8-bit data channels, and additional horizontal and vertical sync (HS/VS), data enable (DE), pixel clock signals (VCLK). User should select the correct signals to connect according to different Video format. VCLK is always needed in any mode. When use 8bit with embedded sync signal (8bit ITU-R BT.656 YCbCr/Mono 4:2:2), only G[7..0] bus and VCLK are needed.

OLED Display receives data with BT601/656 format, like 8/16/24 bits and 4:2:2/4:4:4 format, and video decoder outputs 24 bits RGB signal always, then sends the signal to Video signal enhancement module and output keep 24 bits format. The gamma correction circuit makes corrections of the 24 bit RGB signal by separated RGB look-up table, and extends to 30 bits RGB signal output.

If the input video format is CVBS, component, VGA (analog RGB), HDMI, DVI video signals, etc., OLED Display requires an external video decoder, such as ADV7180, AD9985, ADV7611 and so on.

3.1.1 Input Video Standard

Table 3-1   Input Signal Standard & Pin Used

| Video Standard	Color Space	PIN		
		R[7:0]	G[7:0]	B[7:0]
8-bit, 4:2:2	YCbCr	-	YCbCr[7:0]	-
8-bit, Mono	Y	-	Y[7:0]	-
16-bit, 4:2:2	YCbCr	-	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]
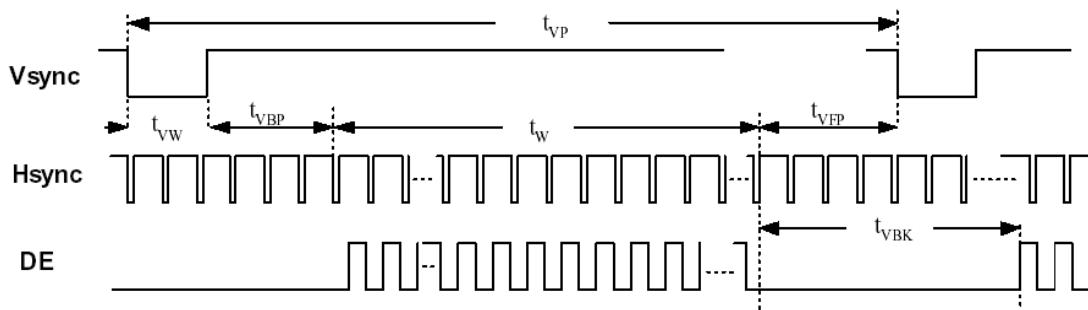
Figure 3-2   Input Sync Signals Timing (For All Formats)
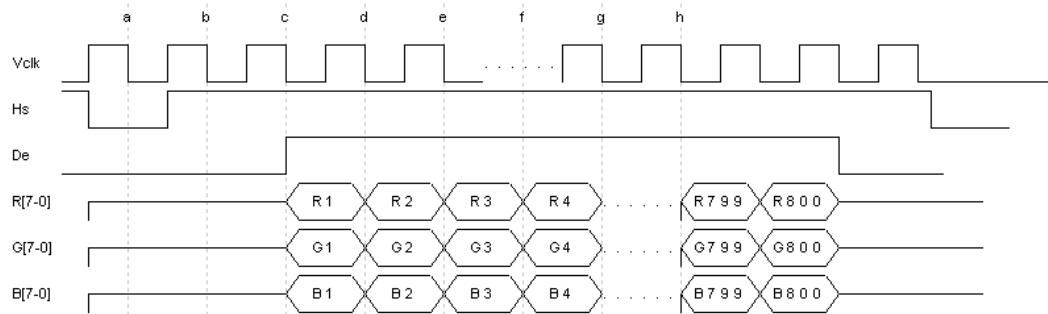
Figure 3-3   24-bit, 4:4:4 RGB Input VideoTiming
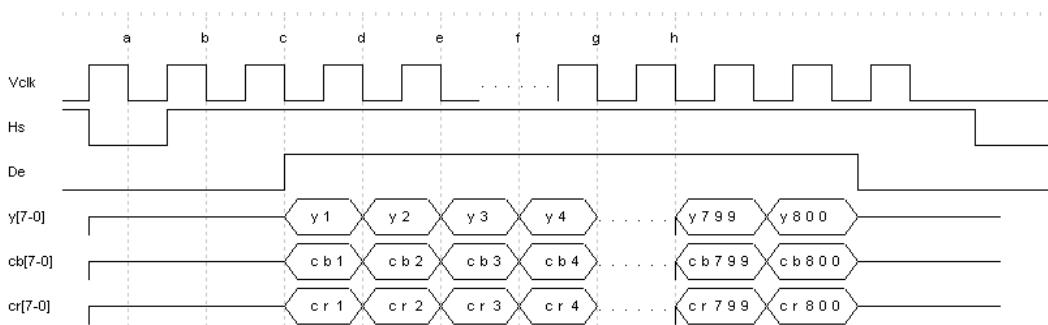

Figure 3-4   24-bit, 4:4:4 YCbCr Input Video Timing
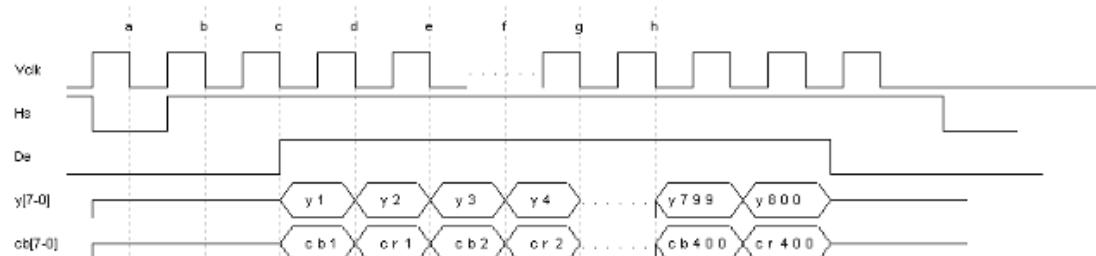

Figure 3-5   16-bit, 4:2:2 YCbCr Input Video Timing
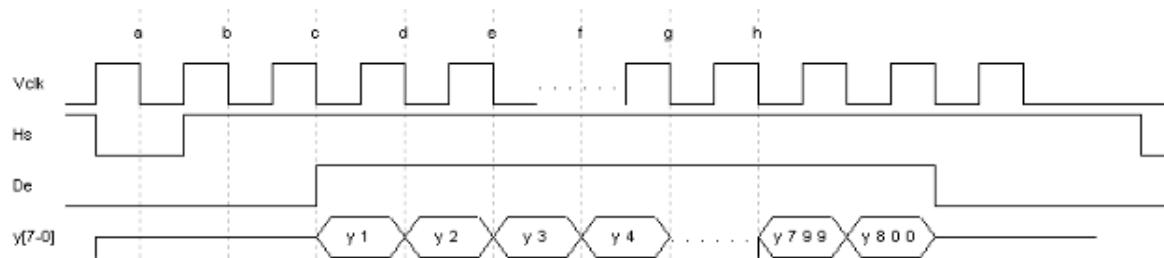

Figure 3-6   8-bit, Mono Input Video Timing
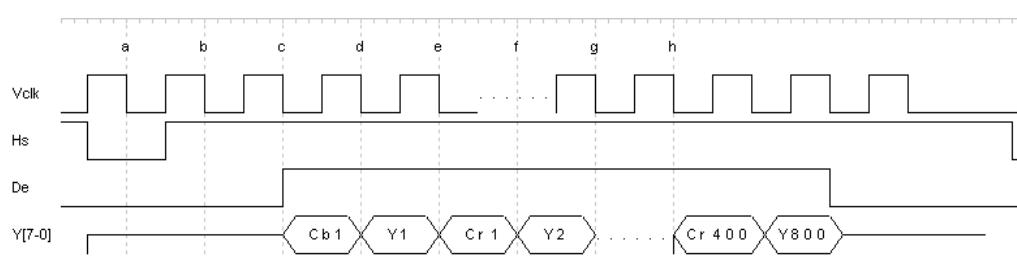
Figure 3-7   8-bit, 4:2:2 YCbCr input Video timing

Table 3-2   VESA Progressive Video Modes

Mode		Frequency	Total	Active	Front Porch + Border	Sync Pulse	Back Porch + Border
SXGA 1280X1024 85Hz non-interlaced	H	91.146 KHz	1728 pixels	1280 pixels	64 pixels	160 pixels	224 pixels
	V	85.024 Hz	1072 lines	1024 lines	1 line	3 lines	44 lines
	P	157.500 MHz					
SXGA 1280X1024 75Hz non-interlaced	H	79.976 KHz	1688 pixels	1280 pixels	16 pixels	144 pixels	248 pixels
	V	75.025 Hz	1066 lines	1024 lines	1 line	3 lines	38 lines
	P	135.000 MHz					
SXGA 1280X1024 60Hz non-interlaced	H	63.981 KHz	1688 pixels	1280 pixels	48 pixels	112 pixels	248 pixels
	V	60.020 Hz	1066 lines	1024 lines	1 line	3 lines	38 lines
	P	108.000 MHz					
XGA 1024X768 85Hz non-interlaced	H	68.677 KHz	1376 pixels	1024 pixels	48 pixels	96 pixels	208 pixels
	V	84.997 Hz	808 lines	768 lines	1 line	3 lines	36 lines
	P	94.500 MHz					
XGA 1024X768 75Hz non-interlaced	H	60.023 KHz	1312 pixels	1024 pixels	16 pixels	96 pixels	176 pixels
	V	75.029 Hz	800 lines	768 lines	1 line	3 lines	28 lines
	P	78.750 MHz					
XGA 1024X768 60Hz non-interlaced	H	48.363 KHz	1344 pixels	1024 pixels	24 pixels	136 pixels	160 pixels
	V	60.004 Hz	806 lines	768 lines	3 line	6 lines	29 lines
	P	65.000 MHz					
SVGA 800X600 85Hz non-interlaced	H	53.674 KHz	1048 pixels	800 pixels	32 pixels	64 pixels	152 pixels
	V	85.061 Hz	631 lines	600 lines	1 line	3 lines	27 lines
	P	56.250 MHz					
SVGA 800X600 75Hz non-interlaced	H	46.875 KHz	1056 pixels	800 pixels	16 pixels	80 pixels	160 pixels
	V	75.000 Hz	625 lines	600 lines	1 line	3 lines	21 lines
	P	49.500 MHz					
SVGA 800X600 60Hz non-interlaced	H	37.879 KHz	1056 pixels	800 pixels	40 pixels	128 pixels	88 pixels
	V	60.317 Hz	628 lines	600 lines	1 line	4 lines	23 lines
	P	40.000 MHz					
VGA 640X480 85Hz non-interlaced	H	43.269 KHz	832 pixels	640 pixels	56 pixels	56 pixels	80 pixels
	V	85.008 Hz	509 lines	480 lines	1 line	3 lines	25 lines
	P	36.000 MHz					
VGA 640X480 75Hz non-interlaced	H	37.500 KHz	840 pixels	640 pixels	16 pixels	64 pixels	120 pixels
	V	75.000 Hz	500 lines	480 lines	1 line	3 lines	16 lines
	P	31.500 MHz					
VGA 640X480 60Hz non-interlaced	H	31.469 KHz	800 pixels	640 pixels	16 pixels	96 pixels	48 pixels
	V	59.940 Hz	525 lines	480 lines	10 line	2 lines	33 lines
	P	25.175 MHz					

Table 3-3   VESA Interlaced Video Modes

Mode		Frequency	Total	Active
SMPTE-170M-1 640X480 Mono 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.27 MHz		
SMPTE-170M-2 800X600 Mono 25Hz interlaced	H	15.625 KHz	1052 pixels	800 pixels
	V	50 Hz Field	312.5 lines	300 lines
	P	16.437 MHz		
NTSC 720X480 Color 30Hz interlaced	H	15.734 KHz	858 pixels	720 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	13.5 MHz		
PAL 720X576 Color 25Hz interlaced	H	15.625 KHz	864 pixels	720 pixels
	V	50 Hz Field	312.5 lines	288 lines
	P	13.5 MHz		
NTSC (Square) 640X480 Color 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.2727 MHz		
PAL (Square) 768X576 Color 25Hz interlaced	H	15.625 KHz	944 pixels	768 pixels
	V	50 Hz Field	312.5 lines	288 lines
	P	14.75 MHz		

Table 3-4   VGA and SXGA Video Timing

| Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	f_{CLK}			216	MHz	SXGA 120Hz
HSYNC Period	t_{HP}	670			t_{CLK}	
HSYNC Pulse Width	t_{HW}	10			t_{CLK}	
HSYNC Back Porch	t_{HBP}	10			t_{CLK}	
Horizontal Valid data width	t_{HV}	640		1280	t_{CLK}	
HSYNC Front Porch	t_{HFP}	10			t_{CLK}	
Horizontal Blank	t_{HBK}	30			t_{CLK}	
VSYNC Period	t_{VP}	243			t_{HP}	
VSYNC Pulse Width	t_{VW}	1			t_{HP}	
VSYNC Back Porch	t_{VBP}	1			t_{HP}	
Vertical valid data width	t_{W}	240		1024	t_{HP}	
Vertical Front Porch	t_{VFP}	1			t_{HP}	
Vertical Blank	t_{VBK}	3			t_{HP}	
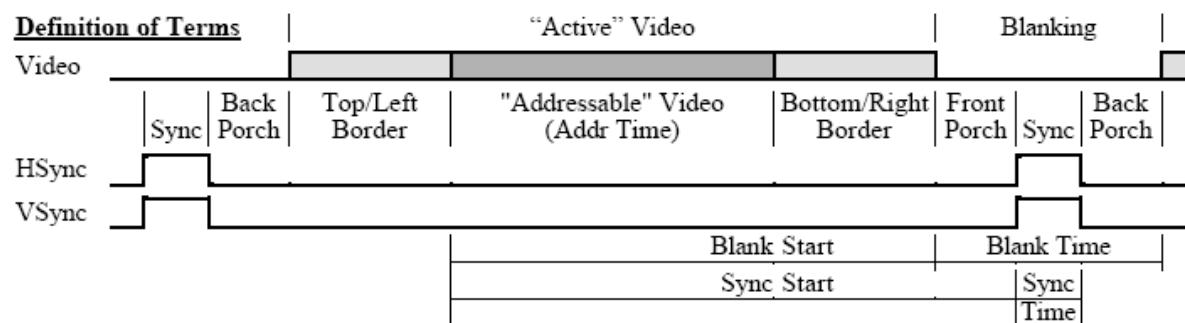
Figure 3-8   VESA Definition of Terms

3.1.2 Color Space

If the input data format is YCbCr, the device will change it to RGB format. Color space conversion block converts color space from YCbCr to RGB and uses the following equations. Output signal is 24-bit RGB format, 8-bit in each path.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$

$$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$

$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$

3.1.3 Digital Video Signal Enhancement

Digital video signal enhancement can be achieved by adjusting the brightness and the contrast ratio, as is shown in Figure 3-9.
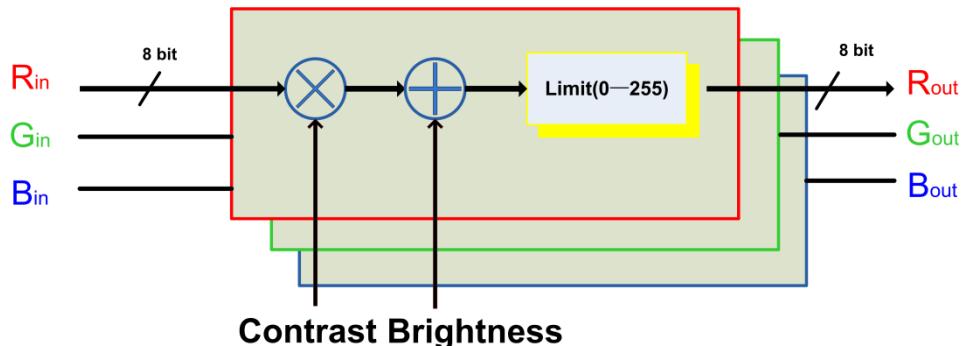

Figure 3-9   Digital Video Signal Enhancement Diagram

Brightness adjustment using addition and subtraction to achieve, the output value is equal to the input value plus the value of register 08H, and then minus 128. When the value of register 08H is greater than 80H, it means increase the brightness, whereas decrease. Brightness adjustment range is ±128.

$$V_{out} = V_{in} + Reg(08H) - 128$$

Contrast adjustment using multiplication and division to achieve, the output value is equal to the input value multiplied by the value of register 09H and then divided by 128. When the value of register 09H is greater than 80H, it means increase the contrast, whereas decrease. The gain of contrast adjustment range is 0 to 2.

$$V_{out} = V_{in} \cdot \frac{Reg(09H)}{128}$$

Note: The algorithms keep only 8bit data, if overflow, automatically discarded high bit.

3.1.4 Video Pattern Generation

Built-in test pattern generator can generate color bars, gray scale, tiles, horizontal stripes, vertical stripes, as well as monochrome red, green, blue, white, black and adjustable any R/G/B gray test pattern. Register 06H is pattern mode selection, default value is 0, indicates the test pattern generator is turned off; when select adjustable R/G/B gray pattern mode, registers 07:08H, 09:0AH and 0B:0CH are used to set the 10-bit gray level of R/G/B channels respectively. Details of setting refer to Table 3-5 and Figure 3-10

Table 3-5   Summary of Test Pattern Setting

Pattern \ Register	Mode (06H)	R (07:08H)	G (09:0AH)	B (0B:0CH)
Color Bar	01H	—	—	—
Gray Scale	02H	—	—	—
Checker Board (40×40)	03H	—	—	—
Alternating every 2 rows	04H	—	—	—
Alternating every 2 columns	05H	—	—	—
All black	06H	—	—	—
All white	07H	—	—	—
All Red	08H	—	—	—
All Green	09H	—	—	—
All Blue	0AH	—	—	—
Adjustable RGB Gray[1]	0BH	0~1023	0~1023	0~1023

Note   ①At adjustable RGB gray mode, the gray level range both are 0~1023 (10-bit) of RGB channels. Two 8-bit registers are used to storing the 10-bit data. The first register (07H/09H/0BH) only the lowest 2-bit are valid for storing the 2 MSB bits of the 10-bit data, and the second register (08H/0AH/0CH) are use to storing the 8 LSB bits.

Color Bar

Gray Scale

Checker Board

Alternating every 2 rows

Alternating every 2 columns
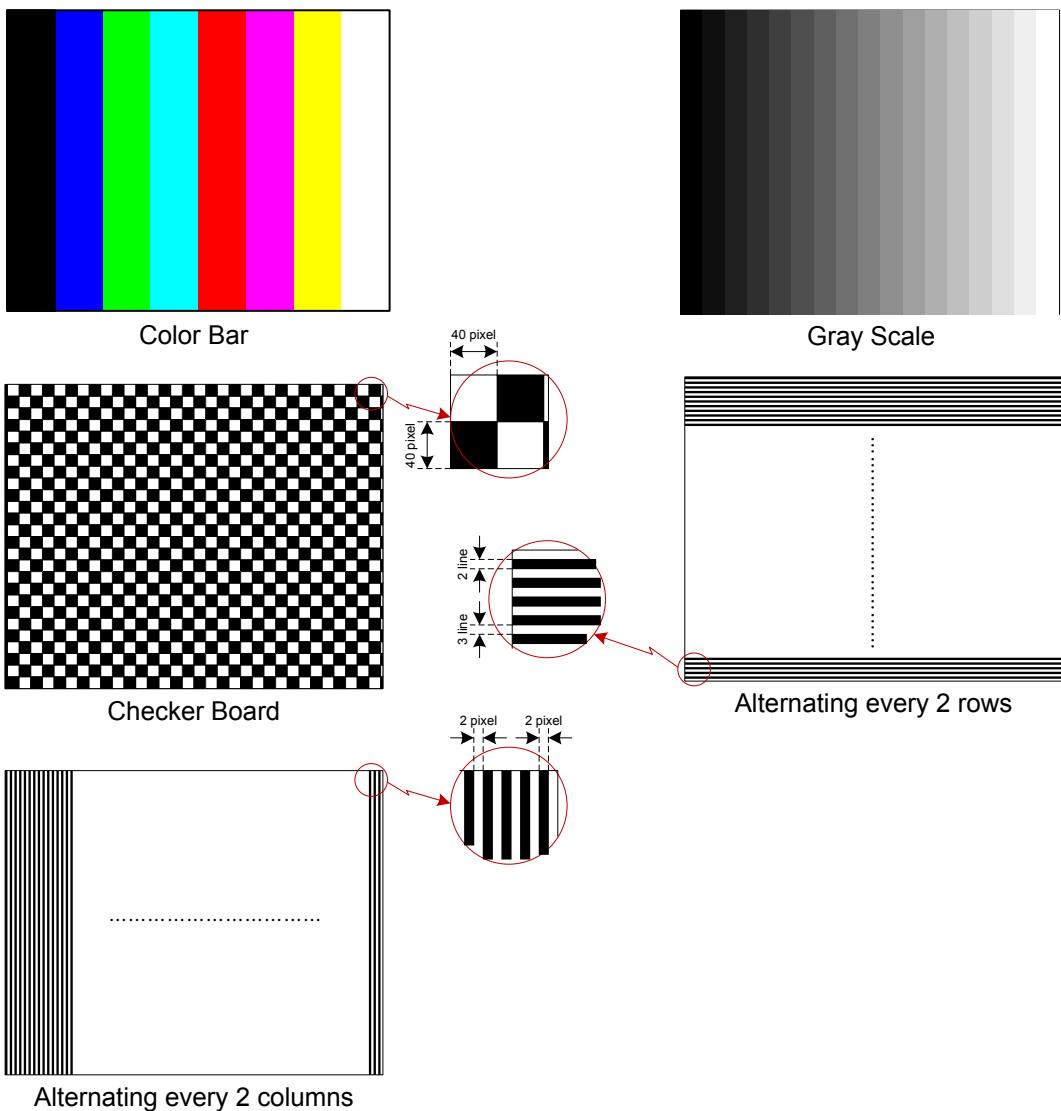
Figure 3-10   Test Video Patterns

3.1.5 Gamma Correction

SXGA series products integrate 3-channel RGB separate lookup table (LUT) to achieve high-precision gamma correction. Each LUT has 256-point, 8-bit input to 10-bit output resolution.

At power-on default state, gamma correction is disabled, the LUTs were filled with random values. 8-bit input video data is directly sent to the MSB of 10-bit output bus, and the low 2-bit is set to 0. User needs to initializes the LUT before enabled the gamma correction, otherwise there might be display irregularly.

The LUT's working is depended on the external input clock signal (VCLK), when the Reset pin is release (set to 1), wait at least 1024 VCLK cycles before to operating the LUT. If no VCLK, the LUT's operating does not have any error response, but the actual operating will not been performed, even to enabled the gamma correction.

The LUT's operating using a register groups and special timing, details refer to section 3.7.3.

3.2 3D Video Display

Register 20H.bit1 used to enable the 3D function and 20H.bit0 used to set the polarity of 3D input signal, cooperated with 3D pin's input (Pin9), the 3D video display can be achieved. If 3D pin's input level is same as the setting of 20H.bit0, the video input is valid, and the frame/field video will be updated, otherwise, video input is invalid and the display will keep the current frame/field. 3D pin's signal is latched at VS falling edge. 3D video display timing is shown in Figure 3-11.

In progressive mode, 3D video signal using frame timing mode, such as the odd frame is updated left display, and the even frame is updated right display.

In interlaced mode, 3D video signal using field timing mode, such as the odd field is updated left display, and the even field is updated right display. At this point, the vertical resolution of each field is lower compare with the source, the bit5 and bit4 of register(02H) should be set to "11", display will repeat to display each line in next line automatically, to ensure that the image aspect ratio and display.
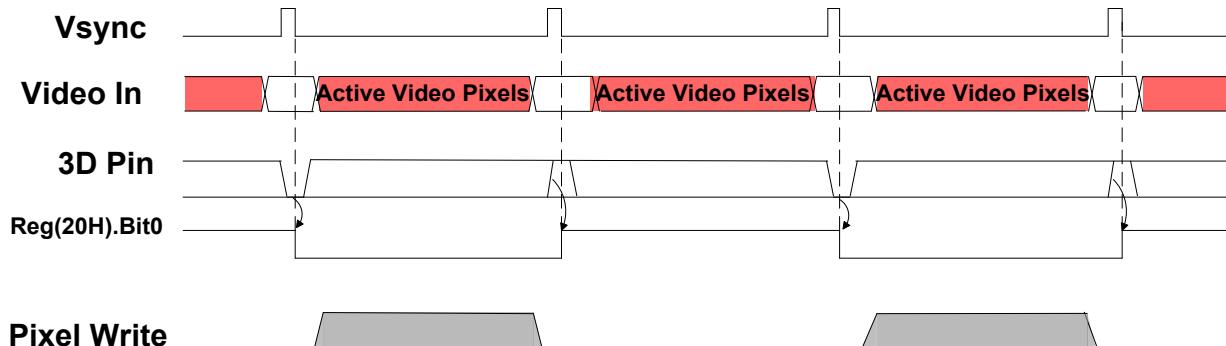

Figure 3-11   3D Video Display Timing

3.3 Power Supply & Reset

SXGA060 only need 5V power supply. Internal LDO will support the 1.8V for digital core. 5V is used for OLED pixels driver, D/A converter and DC-DC module. To ensure the display image quality, please note that ripple and noise rejection of 5V power supply.

3.3.1 Power UP/Down Sequence

The system power-up mechanism relies on the clock signal (VCLK), so the power supply and VCLK input sequence is very important. SXGA060 requires first provide VCLK, followed is 1.8v, and last is 5V. The working principle is shown by following figure and section 3.3.2.

If the power-up sequence cannot meet requirements, SXGA060's working state may abnormal. In that case, after the reset and initialization operations, user can set the PDOWN (Register 40H.Bit7) to 1 first, and wait 20ms, then set PDOWN to 0.
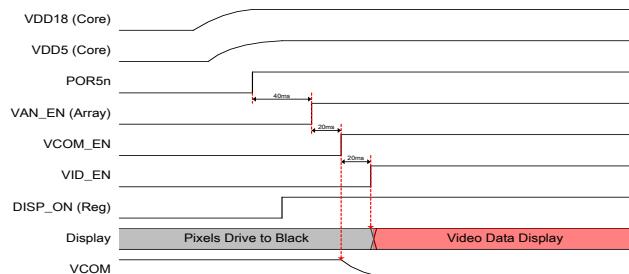
Figure 3-12   Power-up Sequence ($V_{th\_1.8}$=1.2V)
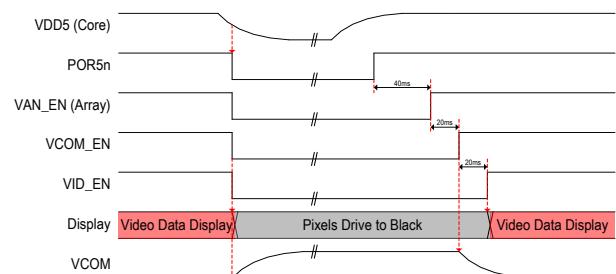

Figure 3-13   V5.0 Power Down & Up (Vth=4V)
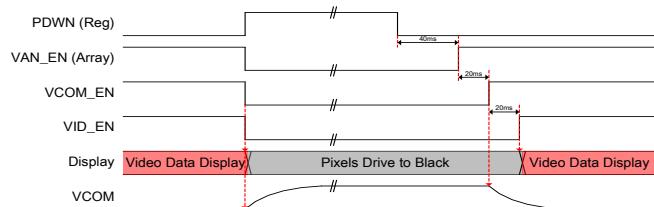
Figure 3-14   Register Control Power Down & Up
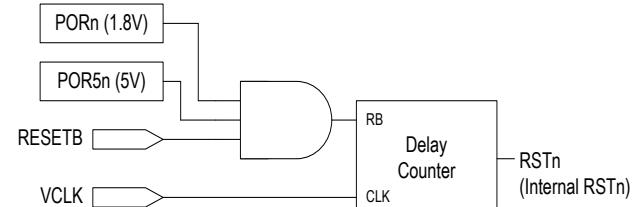

Figure 3-15   Reset Block Diagram

3.3.2 Reset Sequence
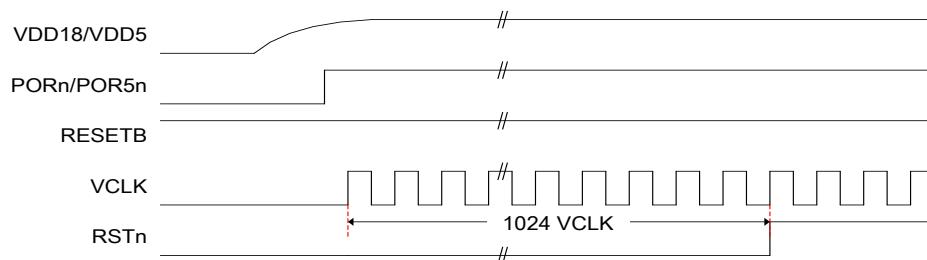


Figure 3-16   Reset Timing Case 1 – No external reset pin used (RESETB=1)
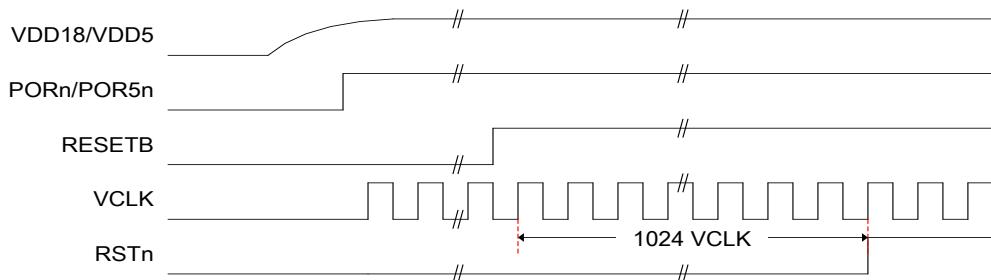
Figure 3-17   Reset Timing Case 2 – External reset pin depend on VCLK
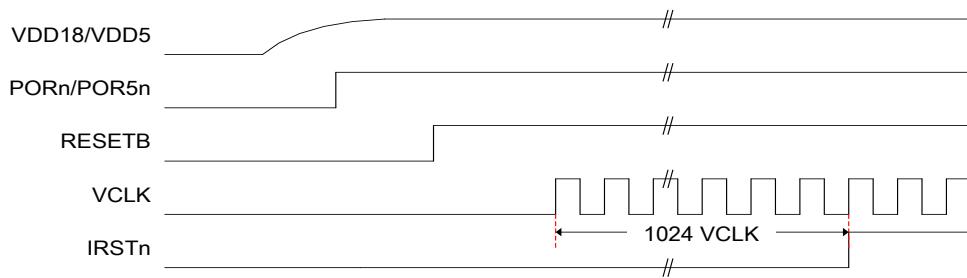
Figure 3-18   Reset Timing Case 3 – External reset pin applied

3.4 Unit Drive Circuit

SXGA060 series AMOLED pixel drive circuit is shown in Figure 3-19. Each OLED light-emitting diodes use voltage-driven approach, the typical photo electric properties is shown in Figure 3-20.

When scanning signals ROWSEL and ROWSWL_B are valid at the same time, signal Video_In charges the capacitance C through MOS transistors P1&N1, and controls the output of N2. The capacitance C can be guaranteed to maintain the output of N2 in a frame/field cycle.

N2 is used in Source-Follower structure to control 5V (Van) power supply, the current flowed through the protection resistor R is applied to the OLED anode.

All pixels cathode of OLED is connected to negative voltage Vcom (common cathode structure), Vcom can be adjusted by set 9-bit registers 34:35H in order to achieve the display brightness adjustment.

N3 is used for discharge of parasitic capacitance of the OLED rapidly, thereby improving dynamic contrast of the display. The discharge enabled by register 21H.bit3.
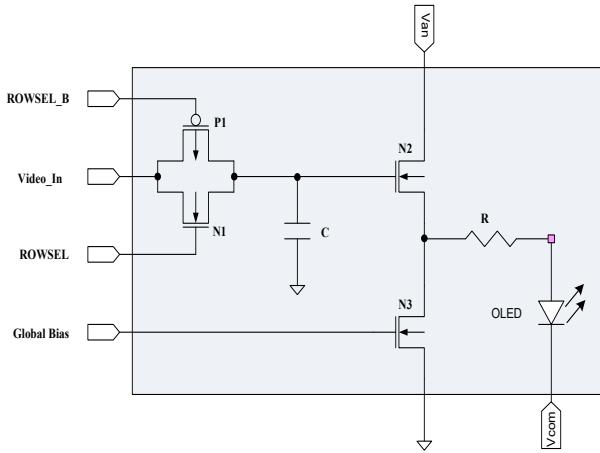
Figure 3-19   Unit Drive Circuit   Figure 3-20   OLED photo electricity properties
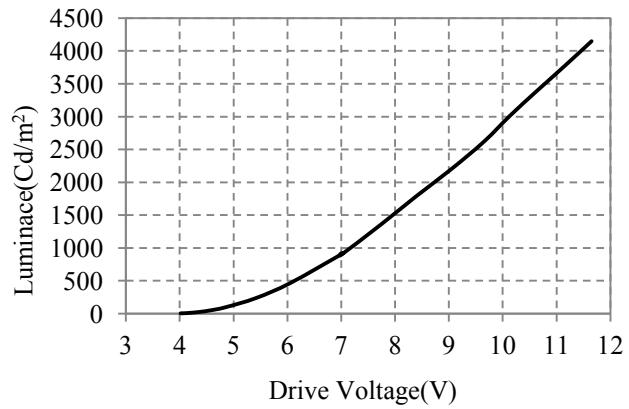
3.5 DC/DC Converter

OLED emitting light needs to be applied positive bias voltage between the anode and cathode, the anode voltage from 5V power supply is controlled by drive transistor, all pixel's common cathode voltage Vcom supplied by DC/DC converter on the PCB backplane. The driving pulse of DC/DC converter is generated by the internal programmable pulse generator, the circuit shown in Figure 3-21. Vcom adjustment range is 0 ~-3V, corresponding to 9-bit registers 34:35H, the typical working curve is shown in Figure 3-22
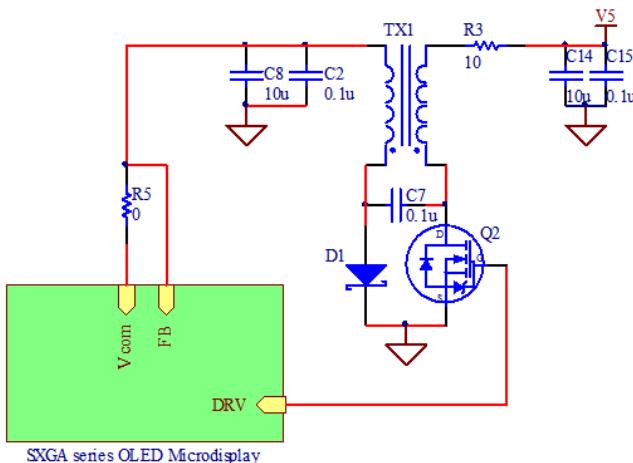
Figure 3-21   DC/DC Principal Diagram   Figure 3-22   Vcom Programmable Working Curve
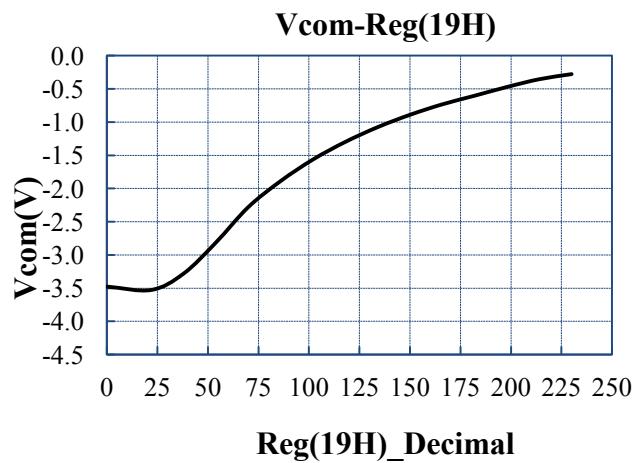
3.6 Temperature Sensor

The working of SXGA060's temperature sensor depend on external VS signal, and the measured value update period is 256 cycles of VS signal (if VS=60Hz, it's about 4.3s).

The value of register 39H is the measured value of internal temperature sensor. So the real-time internal working temperature can be read out through the two-wire serial interface. The temperature value and the readout conversion relation is: $T = 0.47 \times Reg\,(39H) - 40$

The temperature sensor response curve and the calibration curve are shown as Figure 3-26 and Figure 3-27.
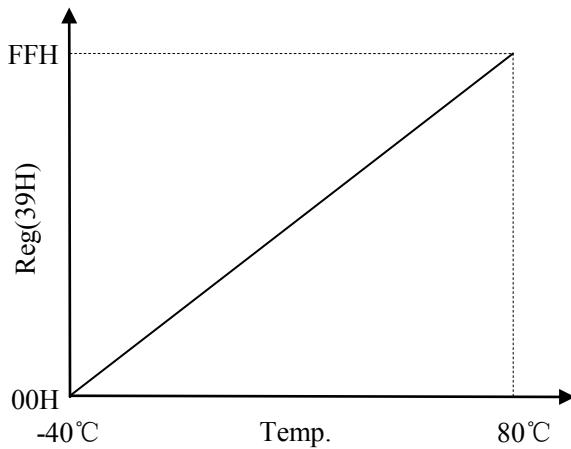
Figure 3-23   Temp. Sensor Readout
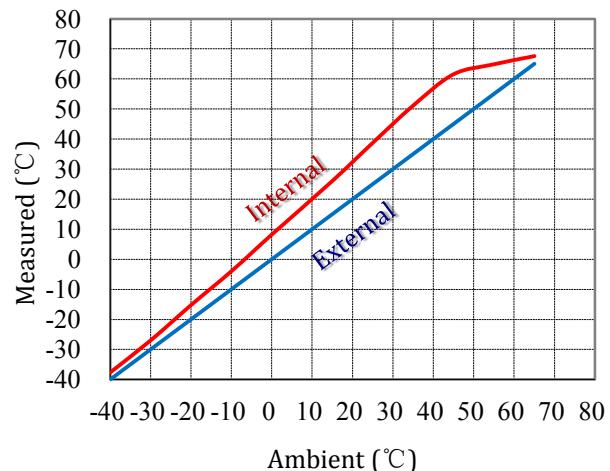
Figure 3-24   Temp. Sensor calibration curve

3.7 Two-wire Serial Interface

SXGA060's two-wire serial interface compatible only with the random address read/write operations of I2C communication standard.

SXGA060 series microdisplay acts as a slave for receiving and transmitting data, all read/write operations must be launched by the master. The SDA and SCL line has been pulled up to internal 1.8v via 10k resistor.

User can realize the display programmable control by use two-wire interface, such as digital video signal decoding and processing, gamma correction, Vcom adjustment and so on.

Key Features and tags of the two-wire serial communication:

1) Communication speed (SCL) support from 100K to 1MHz;
2) 8-bits Slave Address consists of 7-bits device address and 1-bit read/write flag;
3) Start/Re-Start: SDA change from HIGH to LOW while SCL is HIGH, See Figure 3-25;
4) Stop: SDA change from LOW to HIGH while SCL is HIGH, see Figure 3-25;
5) ACK: SDA is LOW during the acknowledge clock pulse;
6) NAK: SDA is HIGH during the acknowledge clock pulse;
7) One transmission includes 8bit data and an acknowledge bit, total nine clock of SCL;
8) Except Start and Stop condition:
   - HIGH or LOW state of SDA can only being changed while SCL is LOW
   - Data on the SDA line must be stable during the HIGH period of the SCL
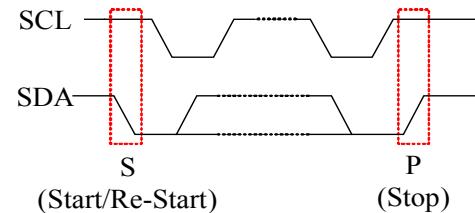
Figure 3-25   Start & Stop Timing

3.7.1 Communication Operating

● Write data (Figure 3-26) :
   1) Master sends Start condition (S)
   2) Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents as low
   3) Slave sends 1bit ACK (A) response
   4) Master sends 8bit register address (Register)
   5) Slave sends 1bit ACK (A) response
   6) Master sends 8bit data (Data)
   7) Slave sends 1bit ACK (A) response
   8) Master sends stop condition(P)

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 3-26   Write Data format

● Read Data (Figure 3-27)
   1) Master sends Start condition (S)
   2) Master sends 7bit Slave Address and 1bit Write flag ($\overline{W}$) represents as low
   3) Slave sends ACK (A) response
   4) Master sends 8bit Register Address (Register)
   5) Slave sends 1bit ACK (A) response
   6) Master sends 1bit Re-Start condition (Sr)
   7) Master sends 7bit Slave Address and 1bit Read flag (R) represents as high
   8) Slave sends 1bit ACK (A) response
   9) Slave sends 8bit Data (Data)
   10) Master sends 1bit NAK ($\overline{A}$) response
   11) Master sends Stop condition (P)

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P
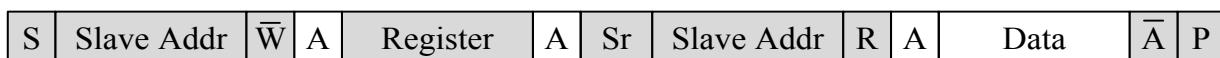
Figure 3-27   Data format (Master reads from Slave)

3.7.2 Serial Interface Bus Address Selection

Two salve address of SXGA060 series microdisplay can be selected by an externally SelAdr0 pin. The SelAdr0 pin has an internal resistor (10K) to pull up to 1.8V power. One of microdisplay's SelAdr0 pin must be connected to GND when used in binocular stereovision application. Microdisplay's corresponding read/write address is shown as Table 3-6.

Table 3-6   Slave Address list

A7 (MSB)	A6	A5	A4	A3	A2	A1 (SelAdr0)	A0 (R/$\overline{W}$)	Slave Address (R/$\overline{W}$)
0	0	0	1	1	1	1(Default)	1/0	1FH/1EH
0	0	0	1	1	1	0	1/0	1DH/1CH

3.7.3 Gamma LUT operation

SXGA060 integrate 3-channel RGB separate lookup table (LUT), and each LUT has 256-point, 10-bit resolutions, so the LUTs addressing rang beyond 8-bit. SXGA060 was using a register groups and special timing to achieve the LUTs operation by indirect addressing mode. The register group definition refers to Table 3-7.

Table 3-7   The register group of Gamma function

Channel	LUT Addressing Register	LUT Data Register		Control Register(10H)		
		MSB_Data[9:8]	LSB_Data[7:0]	En	Read	Update
R	11H	12H	13H		Bit5	Bit2
G	14H	15H	16H	Bit6	Bit4	Bit1
B	17H	18H	19H		Bit3	Bit0

- Write LUT (Example as R channel)
    1) Check 10H.Bit5 = 0;
    2) Initialiation the gamma correction RedData(0~255),   Addr=0;
    3) Write the Addr to 11H;
    4) Write RedData(Addr)_[9:8] to 12H;
    5) Write RedData(Addr)_[7:0] to 13H;   //means: LUT_Red[Addr] = RedData(Addr)
    6) Addr=Addr+1;
    7) repeat 3~6, until Addr=256;
    8) Set 10H.Bit2=1;   //Updating the LUT_Red

  * After 3-channel (RGB) has been updating, set 10H.Bit6 to enable the gamma correction.

- Read LUT (Example as R channel)
    1) Check 10H.Bit5 = 0;
    2) Define arrays ready to receive data;   //RData(256)
    3) Addr=0;
    4) Write Addr to 11H
    5) Set 10H.Bit5=1;   //Start Reading
    6) wait 10H.Bit5=0;   //Data Ready
    7) Read 12H to RData(Addr)_[9:8];
    8) Read 13H to RData(Addr)_[7:0];   // Get RData(Addr)
    9) Addr=Addr+1;
    10) Repeat 4~9, until Addr=256;

4 REGISTER DESCRIPTION

4.1 Summary of Registers

Table 4-1   Summary of Registers

Register	Bytes	Description	Default Value
00H	1	Chip's Revision	10H
01H	1	VCLK and Sync Mode Setting	03H
02H	1	Video Mode Setting	43H
03H	1	Vertical Blank Lines Setting	00H
04H	1	Horizontal Blank Pixels Setting	00H
05H	1	Reserved	-
06H	1	Test Pattern Enable and Mode Setting	00H
07:08H	2	R Channel 10-bit Gray Setting for Pattern Mode(0BH)	000H
09:0AH	2	G Channel 10-bit Gray Setting for Pattern Mode(0BH)	000H
0B:0CH	2	B Channel 10-bit Gray Setting for Pattern Mode(0BH)	000H
0DH	1	Reserved	-
0EH	1	Video Signal Brightness Control	80H
0FH	1	Video Signal Contrast Control	80H
10H	1	Video Coding and Gamma Function Control	40H
11H	1	R Channel LUT Addressing Register	00H
12:13H	2	R Channel 10-bit Correction Data Register	000H
14H	1	G Channel LUT Addressing Register	00H
15:16H	2	G Channel 10-bit Correction Data Register	000H
17H	1	B Channel LUT Addressing Register	00H
18:19H	2	B Channel 10-bit Correction Data Register	000H
1AH~1FH	6	Reserved	-
20H	1	3D Function Control	00H
21H	1	Display On, 2× Zoom and Scanning Direction Control	40H
22:23H	2	Left Margin 9-bit Register	002H
24:25H	2	Right Margin 9-bit Register	002H
26:27H	2	Top Margin 9-bit Register	002H
28:29H	1	Bottom Margin 9-bit Register	002H
30H	1	DAC Offset Control	80H
31H	1	DAC Current Control	44H
32H	1	DAC Function Control	87H
33H	1	DC/DC Function Control	42H
34:35H	2	Vcom 9-bit Setting	1FFH
36H~38H	3	Reserved	-
39H	1	Temperature Output Value	xxH
3AH~3FH	6	Reserved	-
40H	1	Power Down Mode Control	00H

4.2 Detailed Information of Register

Category	Register	R/W	Bit	Function	Default	Description
Revision	00H	R	7:4	Product	0001b	0001b : SXGA
			3:0	Revision	0000b	0000b : Revision Number
Input Video Control	01H	R/W	7	DDRMode	0b	0b : SDR
						1b : DDR
			6	DDR Swap	0b	0b : 1st Data Start at VCLK Falling Edge
						1b : 1st Data Start at VCLK Rising Edge
			5	Field Swap	0b	0b : Normal Field Sync
						1b : Inverted Field Sync
			3	Vsync Polarity	0b	0b : Active Low
			2	Hsync Polarity	0b	1b : Active High
			1:0	Sync Mode	11b	00b : Embedded Sync
						10b : External Sync without DE
						11b : External Sync wity DE
Input Video Control	02H	R/W	7:6	SAV Offset	01b	00b : 1 Pixel before Input SAV
						01b : Same as Input SAV
						10b : 1 Pixel after Input SAV
						11b : 2 Pixel after Input SAV
			5:4	Interlace Mode	00b	00b : Progressive
						10b : Interlaced
						11b : Pseudo-Interlaced (for Field 3D)
			3	DAC CLK Mode	0b	0b : VCLK / 2
						1b : Same as VCLK
			2:0	Data Mode	011b	000b : 16-bit 422 YCbCr
						001b : 24-bit 444 YCbCr
						010b : 8-bit Mono
						011b : 24-bit 444 RGB
						100b : 8-bit 422 YCbCr
	03H	R/W	7:0	V Blank	00H	Vertical Blank Lines
	04H		7:0	H Blank	00H	Horizontal Blank Pixels
Test Pattern Control	06H	R/W	3:0	Test Pattern Mode	0H	0H : Normal (Test Pattern Closed)
						1H : Color Bar
						2H : Gray Scale
						3H : Checker Board (40×40)
						4H : Alternating every 2 Rows
						5H : Alternating every 2 Columns
						6H : All Black
						7H : All White
						8H : All Red
						9H : All Green
						AH : All Blue
						BH : Adjusted R/G/B (Any Gray Level)

Category	Register	R/W	Bit	Function	Default	Description
RGB Gray for Pattern(0BH)	07H	R/W	1:0	TP Red [9:8]	00b	R Channel 10-bit Gray Value
	08H		7:0	TP Red [7:0]	00H	
	09H		1:0	TP Green [9:8]	00b	G Channel 10-bit Gray Value
	0AH		7:0	TP Green [7:0]	00H	
	0BH		1:0	TP Red [9:8]	00b	B Channel 10-bit Gray Value
	0CH		7:0	TP Red [7:0]	00H	
Video Enhancement	0EH	R/W	7:0	Brightness	80H	00H : Darkest 80H : No Change FFH : Brightest
	0FH	R/W	7:0	Contrast	80H	00H : Black Screen 80H : No Change FFH : Double Contrast
Gamma Function Control	10H	R/W	7	Gray Code	0b	0b : Binary Code 1b : Gray Code
			6	LUTs Bypass	1b	0b : Gamma Control Enable 1b : Gamma Control Disable
			5	R LUTs Read	0b	0b : Read Done 1b : Read Start (Automatic Clear after Read)
			4	G LUTs Read	0b	
			3	B LUTs Read	0b	
			2	R LUTs Update	0b	0b : Update Done 1b : Update Start (Automatic Clear after Update)
			1	G LUTs Update	0b	
			0	B LUTs Update	0b	
Gamma LUTs Control	11H	R/W	7:0	R _LUTs_ Address	00H	Read/Write Address for Red Gamma LUTs
	12H		1:0	R_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Red Gamma LUTs
	13H		7:0	R_LUTs_Data[7:0]	00H	
	14H		7:0	G _LUTs_ Address	00H	Read/Write Address for Green Gamma LUTs
	15H		1:0	G_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Green Gamma LUTs
	16H		7:0	G_LUTs_Data[7:0]	00H	
	17H		7:0	B _LUTs_ Address	00H	Read/Write Address for Blue Gamma LUTs
	18H		1:0	B_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Blue Gamma LUTs
	19H		7:0	B_LUTs_Data[7:0]	00H	
3D Function	20H	R/W	1	3D Mode	0b	0b : Disable 1b : Enable
			0	3D Polarity	0b	0b : Active when 3D pin is High 1b : Active when 3D pin is Low
Display Control	21H	R/W	7	Display On	0b	0b : Display Off 1b : Display On
			4	Discharge	1b	0b : Disable 1b : Enable
			3	Column 2×	0b	0b : Disable 1b : Enable (1 Col/Row expand to 2 Col/Rows)
			2	Row 2×	0b	
			1	Horizontal Mirror	0b	0b : Disable (Left to Right, Top to Bottom)

Category	Register	R/W	Bit	Function	Default	Description
			0	Vertical Mirror	0b	1b : Enable (Right to Left, Bottom to Top)
Display Position Control	22H	R/W	0	Left Margin [8]	0b	Display Left Margin [8:0]
	23H		7:0	Left Margin [7:0]	02H	
	24H		0	Right Margin [8]	0b	Display Right Margin [8:0]
	25H		7:0	Right Margin [7:0]	02H	
	26H		0	Top Margin [8]	0b	Display Top Margin [8:0]
	27H		7:0	Top Margin [7:0]	02H	
	28H		0	Bottom Margin [8]	0b	Display Bottom Margin [8:0]
	29H		7:0	Bottom Margin [7:0]	02H	
DAC Control	30H	R/W	7:0	DAC Offset	80H	00H : -40% 80H : 0% FFH : +40%
	31H	R/W	6:4	DAC Current	100b	Adjust DAC Current
			2:0	DAC Buffer Current	100b	Adjust DAC Buffer Current
	32H	R/W	7:6	DAC CLK Delay	10b	00b : -1 VCLK 01b : -1/2 VCLK 10b : Normal 11b : +1/2 VCLK
			5	DAC Output	0b	0b : Disable 1b : Enable
			4	DAC Fly Speed	0b	0b : Slow 1b : Fast
			3	Test	0b	0b : Disable 1b : Enable
			2:0	Dummy Load	111b	000b : Disable 111b : Enable
DC-DC Control	33H	R/W	7	DC-DC CLK	0b	0b : VCLK 1b : Internsal OSC
			6:4	DC-DC Duty	100b	000b : 1:7 001b : 2:6 010b : 3:5 011b : 4:4 100b : 5:3 101b : 6:2 110b : 7:1
			3	DC-DC Driver 2×	0b	0b : Normal 1b : 2× Driver

Category	Register	R/W	Bit	Function	Default	Description
			2:0	DC-DC Divide	010b	000b : 8 001b : 16 010b : 32 011b : 64 100b : 128 101b : 256 110b : 512 111b : 1024
Vcom Setting	34H	R/W	0	VcomLevel [8]	1b	Programble Vcom Level [8:0]
	35H		7:0	VcomLevel [7:0]	FFH	
Temperature	39H	R	7:0	Temperature Value	0～FFH	Temperature Output Value
Power Down Mode	40H	R/W	7	All	0b	0b : Normal 1b : Power-Down
			3	DAC	0b	
			2	DAC Buffer	0b	
			1	DC-DC	0b	
			0	Temperature Sensor	0b	

4.3 Register Setting Examples

4.3.1 24 bit 444 RGB Mode

Register	Setting	Description
01H	02H	SDR Mode, VCLK Falling, Polarity is High, External Sync Without DE
02H	4BH	Same as SAV, Progressive, DAC CLK=VCLK, 24Bit 444 RGB
03H	27H	V_Blank =39
04H	96H	H_Blank = 150
22:23H	002H	Left Margin = 2
24:25H	002H	Right Margin = 2
25:26H	002H	Top Margin = 2
27:28H	002H	Bottom Margin = 2
32H	A0H	DAC Setting
34:35H	0F0H	Vcom Setting
21H	80H	Display On, Mirror Disable

4.3.2 Display Position Setting

Left Margin = Right Margin   = $(1284 - X\_Resolution) / 2$

Top Margin = Bottom Margin   = $(1028 - Y\_Resolution) / 2$

Table 4-2   Display Position Setting Example

Video Mode				Register Setting					
Mode	Scan	Input	Display	Reg(01H)	Reg(07H)	Reg(11h)	Reg(12H)	Reg(13H)	Reg(14H)
SXGA	Progressive	800×600	800×600	3CH	00H	02H	02H	02H	02H
VGA	Progressive	640×480	640×480	3CH	00H	52H	52H	52H	3EH
SMPTE-170M-1	Interlaced	640×480	640×480	21H	00H	52H	52H	52H	3EH
SMPTE-170M-2	Interlaced	800×600	800×600	3DH	00H	02H	02H	02H	02H
NTSC	Interlaced	720×480	640×480	41H	04H	52H	52H	52H	3EH
PAL	Interlaced	720×480	640×480	41H	05H	52H	52H	52H	3EH
NTSC (SQ)	Interlaced	640×480	640×480	41H	00H	52H	52H	52H	3EH
PAL (SQ)	Interlaced	768×676	768×576	41H	00H	12H	12H	14H	0EH

5 MECHANICAL CHARACTERISTICS

5.1 Mechanical Drawing

Pixel(1,1)

13.90 +0.5 -0
9.50±0.1
0.55±0.05
1.44±0.1

Display Center

9.56
10.50±0.1
11.60±0.1
11.67±0.02
17.00±0.15

7.01
11.94
12.90±0.1
15.08±0.02
22.00±0.15

1.80 +0 -0.5

0.80±0.05
0.05±0.02
0.06±0.03
1.15±0.15
1.76±0.15

6
5

Zoom A

Zoom A
5:1

4.7
2.3

4   3   2   1

Pin_1 Mark

6	Adhesive	Scale	OLiGHTEK Co., Ltd.		
5	OLED Layer & Adhesive	3.2:1			
4	Wirebond Encap		Title	SXGA060 Assembly Drawing	
3	Glass Cover				
2	Si-Base Sub		Designed	ZHQ	Version	V1.0
1	PCB Backboard		Checked	YXH	Date	Jul 18, 2013
Item	Name		Approved	LYW	Sheets	1/1

5.2 PCB Backboard Schematic
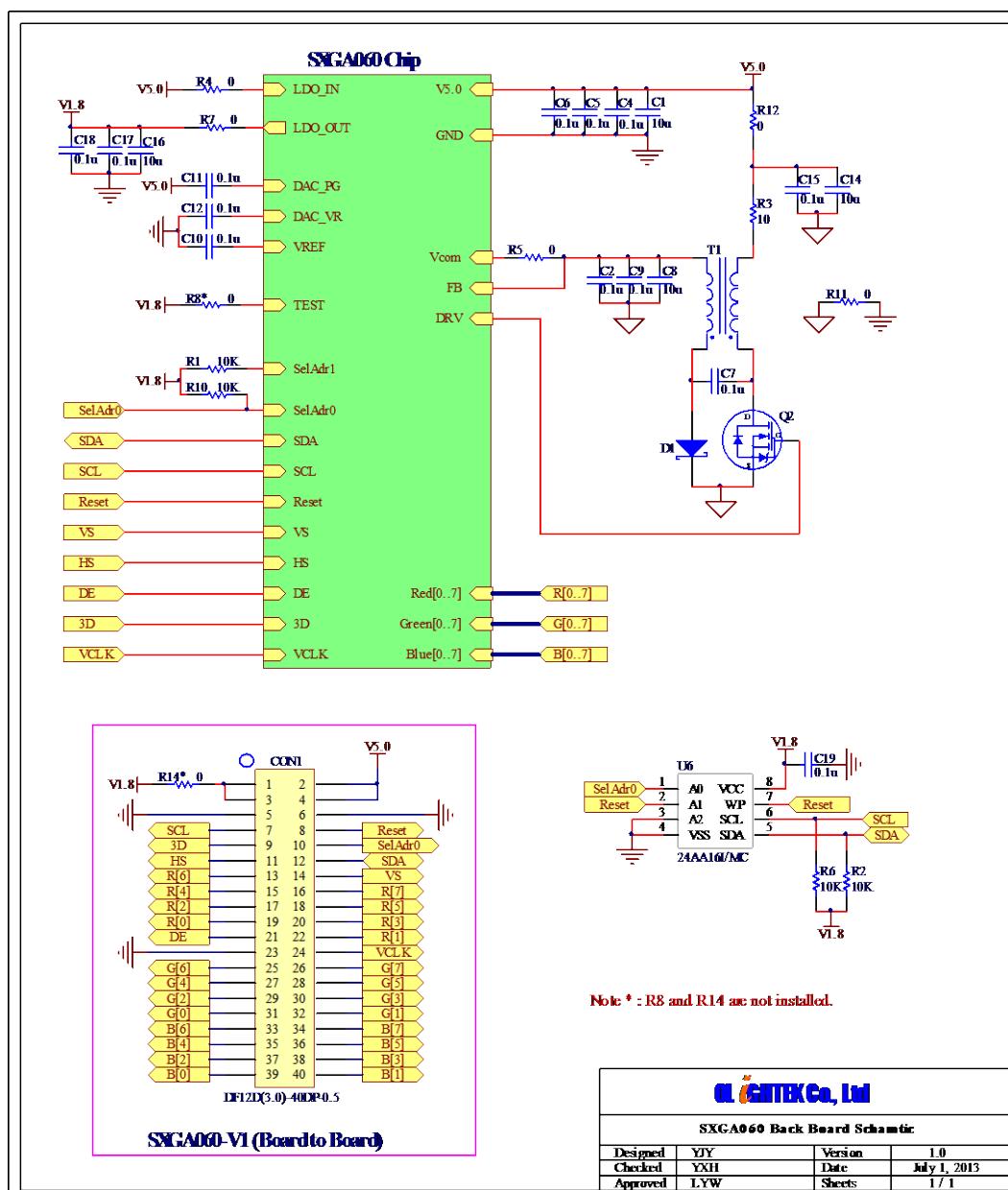
5.3 Assembly Bill of Materials

Item	Type	Reference	Qty	Description	Coding	Manufacturer
1	CAP	C2,C4,C5,C6,C7,C9,C10, C11,C12,C15,C17,C18,C19	13	Cap, 0.1μF/25V, X5R, 0402	TMK105BJ104KV-T	TAIYO YUDEN
		C1,C8,C14,C16	4	Cap, 10μF/16V, X5R, 0603	EMK212BJ106KG-T	TAIYO YUDEN
2	Diode	D1	1	Schottky Diode, 30V/1.5A, SOD323F	PMEG3015EJ	PHILIPS
3	Connector	Con1	1	Connector, 40Pin, 0.5mm, Header	DF12D(3.0)-40DP-0.5V	Hirose
4	n-FET	Q2	1	nFET, 25V/0.22A, SOT-23	FDV301N	Fairchild
5	Resistor	R1,R2,R6,R10	4	Resistor, 10K, 5%, 1/16W, 0402	RC0402JR-0710KL	Yageo
		R3	1	Resistor, 10Ω, 5%, 1/4W, 0805	RC0805JR-0710RL	YAGEO
		R4,R5,R7,R8,R11,R12,R14	7	Resistor, 0Ω, 5%, 1/16W, 0402	RC0402JR-070RL	YAGEO
6	Transformer	TX1	1	Transformer, 6.8μH/0.6A, 1:1	LPD4012-682ML	Coilcraft
7	EEPROM	U6	1	2K I2C Serial EEPROM, DFN-8	24AA02	Microchip

6 PRODUCTS CLEANING, HANDLING AND STORAGE

6.1 Cleaning

- Avoid using any acid, alkali and organic solvent to clean or contact to the display
- Using the lens paper or clean cloth to clean the surface is recommend

6.2 General Handling Considerations

- Do not expose the display to strong acids, alkalis, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation.
- Do not using sharp objects to contact the glass and silicon regions of display.
- Avoid applying force to the any region except the PCB backplane, especially apply the force to the region of sealing, silicon edge and cover glass is not allowed.
- Avoid immersion of the display in any liquid.
- Handing with PVC clean gloves is recommended.

6.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge due to integrated CMOS circuit in the display. The following measures are recommended to minimize ESD occurrences:

- Operate on a region which is equipped with electro-static eliminator, such as ionizing air blowers.
- Wear the anti-static wrist strap
- wear the non-chargeable clothes
- Keep away from charged region.

Figure 6-1   Handing the Display

6.4 Storage

6.4.1 Short Term Storage

The display should be stored in a dry environment with temperature range from -50℃ to 90℃ for a short period(≤100hrs).

6.4.2 Long Term Storage

If the display is stored in such an environment with excessive heat or cold or moisture, the lifetime of display will be shorten, even the environment can cause permanent damage to the display. Recommended long-term storage condition as follows:

- Room temperature: 25℃±5℃
- Dry environment: dry nitrogen or vacuum sealing cabinet
- Static placing: avoid violent vibration

7 APPENDIX

7.1 List of Figures

7.2 List of Tables